WHAT IS CLAIMED IS:

1. A backplane, comprising:

a front side portion having a plurality of front connector holes organized into a set of standardized front connector segments; and

a rear side portion having a plurality of rear connector holes organized into a set of rear connector segments that substantially correspond to said front connector segments,

wherein at least one rear connector segment includes a set of non-standard rear connector holes that are in addition to said at least one rear connector segment's rear connector holes organized into a standardized form such that said set of non-standard rear connector holes are operable to support a signal pathway independent of a standard bus path supported by at least one of said standardized front connector segments.

2. The backplane as set forth in claim 1, wherein said set of standardized front connector segments and said set of rear connector segments comprise five connector segments each, said connector segments conforming to the Compact Peripheral Component Interconnect (CPCI) standard.

3. The backplane as set forth in claim 1, wherein said signal pathway supported by said set of non-standard rear connector holes of said at least one rear connector segment comprises a proprietary input/output (I/O) bus system.

4. The backplane as set forth in claim 1, wherein said front connector holes of said standardized front connector segments and said rear connector holes of said corresponding rear connector segments are coupled together so as to form through-holes.

5. The backplane as set forth in claim 1, wherein said signal pathway supported by said set of non-standard rear connector holes of said at least one rear connector segment is operable to carry at least one user-defined signal.

6. The backplane as set forth in claim 1, wherein said set of standardized front connector segments and said set of rear connector segments conform to one of the VME and Eurocard standards.

7. The backplane as set forth in claim 1, wherein said set of standardized front connector segments and said set of rear connector segments conform to the MultiBus standard.

8. The backplane as set forth in claim 1, wherein said set of non-standard rear connector holes of said at least one rear connector segment comprises at least one column of connector holes.

9. A method for introducing user-defined signals into a Compact Peripheral Component Interconnect (CPCI)-compliant backplane, comprising the steps:

providing a front side portion of said backplane with a plurality of front connector holes that are organized into a set of standardized front connector segments, wherein at least one of said standardized front connector segments is operable to support a CPCI-compliant bus for carrying CPCI signals; and

providing a rear side portion of said backplane with a plurality of rear connector holes that are organized into a set of rear connector segments which substantially correspond to said front connector segments, wherein at least one rear connector segment includes a set of non-standard rear connector holes that are in addition to said at least one rear connector segment's rear connector holes organized into a standardized form such that said set of non-standard rear connector holes are operable to support a signal pathway independent of said CPCI-compliant bus.

10. The method for introducing user-defined signals into a CPCI-compliant backplane as set forth in claim 9, wherein said signal pathway supported by said set of non-standard rear connector holes of said at least one rear connector segment is operable to carry at least one user-defined signal.

11. The method for introducing user-defined signals into a CPCI-compliant backplane as set forth in claim 10, said wherein at least one user-defined signal comprises a Super Frame Indicator (SFI) signal operable to control the operation of a telecommunications rack in which said backplane is deployed.

12. The method for introducing user-defined signals into a CPCI-compliant backplane as set forth in claim 10, said at least one user-defined signal comprises an Extended Alarm Signal (EAS) operable to carry a plurality of alarms generated in the operation of a telecommunications rack in which said backplane is deployed.

13. A connector system, comprising:

a Compact Peripheral Component Interconnect (CPCI)-compliant backplane having a plurality of slots, each slot including five front side connector segments (denoted herein as P1 through P5) and five rear side connector segments (denoted herein as rP1 through rP5) that substantially correspond to said front side connector segments, wherein at least one of said P1 and P2 connector segments is operable to support a CPCI-compliant bus and further wherein at least one of said rP1 and rP2 connector segments is provided with a set of non-standard connector holes in addition to standard rear connector holes;

a front side card coupled to said backplane at a particular slot, said front side card operating to carry a plurality of CPCI signals via said CPCI-compliant bus formed to interconnect said P1 and P2 connector segments of said slots; and

a rear side card coupled to said backplane at said particular slot's rear side connector segments, said rear side card operating to carry at least one user-defined signal via a rear side backplane bus formed to interconnect said non-standard connector holes of said rP1 and rP2 connector segments of said slots.

14. The connector system as set forth in claim 13, wherein said at least one user-defined signal is provided from said rear side card to said front side card via a coupling between said P3 and rP3 connector segments.

15. The connector system as set forth in claim 13, wherein said at least one user-defined signal is provided from said rear side card to said front side card via a coupling between said P4 and rP4 connector segments.

16. The connector system as set forth in claim 13, wherein said at least one user-defined signal is provided from said rear side card to said front side card via a coupling between said P5 and rP5 connector segments.

17. The connector system as set forth in claim 13, wherein said at least one user-defined signal comprises a Super Frame Indicator (SFI) signal operable to control the operation of a telecommunications rack in which said backplane is deployed.

18. The connector system as set forth in claim 13, wherein said at least one user-defined signal comprises an Extended Alarm Signal (EAS) operable to carry a plurality of alarms generated in the operation of a telecommunications rack in which said backplane is deployed.

19. The connector system as set forth in claim 13, wherein said P1 and P2 connector segments are formed as a monoblock.

20. The connector system as set forth in claim 13, wherein said P4 and P5 connector segments are formed as a monoblock.

21. The connector system as set forth in claim 13, wherein said non-standard rear connector holes are dimensioned to receive ultrashort press-in pins formed at a corresponding connector portion of said rear side card.

22. A backplane, comprising:

a front side portion having a plurality of front connector holes organized into a set of front connector segments; and

a rear side portion having a plurality of rear connector holes organized into a set of rear connector segments that substantially correspond to said front connector segments,

wherein at least one of said front connector segments and said rear connector segments includes a set of non-standard connector holes that are in addition to standard connector holes forming said at least one connector segment such that said set of non-standard connector holes are operable to support a signal pathway independent of a standard bus path supported by at least one standard front connector segment.

23. The backplane as set forth in claim 22, wherein said set of front connector segments and said set of rear connector segments comprise five connector segments each, said connector segments conforming to the Compact Peripheral Component Interconnect (CPCI) standard.

24. The backplane as set forth in claim 22, wherein said signal pathway supported by said set of non-standard rear connector holes of said at least one rear connector segment comprises a proprietary input/output (I/O) bus system.

25. The backplane as set forth in claim 22, wherein said signal pathway supported by said set of non-standard connector holes of said at least one of said front connector segments and said rear connector segments is operable to carry at least one user-defined signal.

26. The backplane as set forth in claim 22, wherein said set of front connector segments and said set of rear connector segments conform to one of the VME and Eurocard standards.

27. The backplane as set forth in claim 22, wherein said set of front connector segments and said set of rear connector segments conform to the MultiBus standard.

28. The backplane as set forth in claim 22, wherein said set of non-standard connector holes of said at least one of said front connector segments and said rear connector segments comprises at least one column of connector holes.

29. The backplane as set forth in claim 22, wherein said set of non-standard connector holes of said at least one of said front connector segments and said rear connector segments are dimensioned to receive ultrashort CPCI-compliant pins.